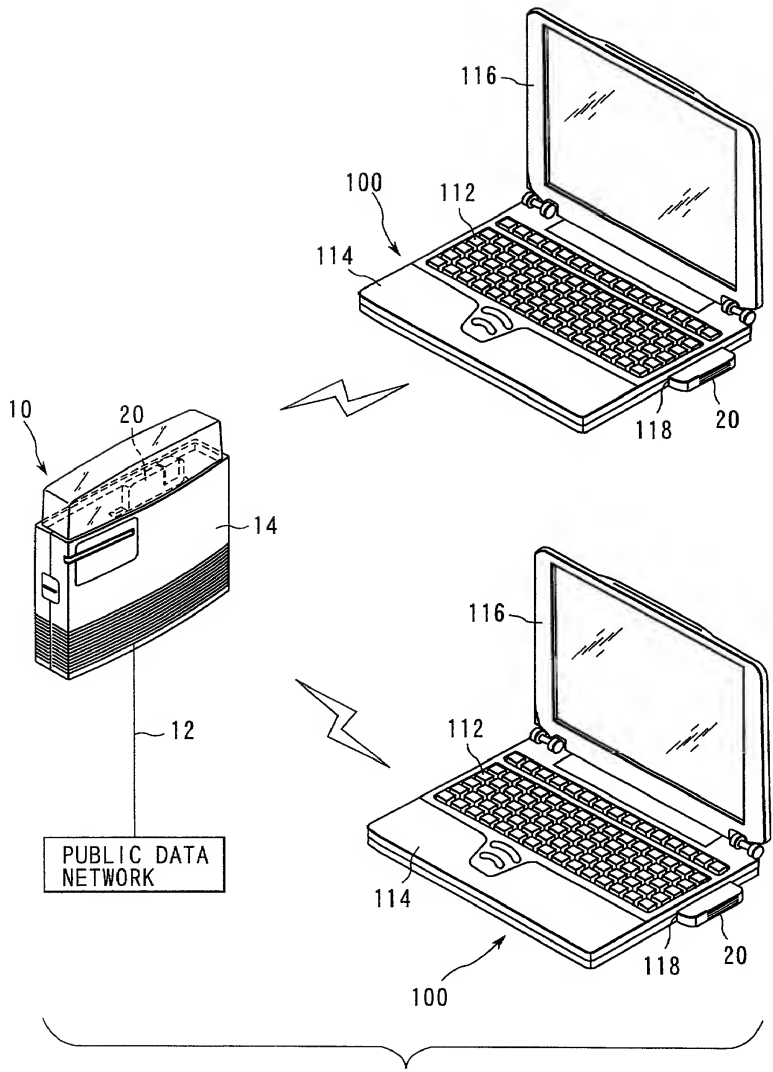
116
100
112
114
118
20
10
20
14
12
PUBLIC DATA NETWORK
116
112
114
118
20
100

FIG. 1

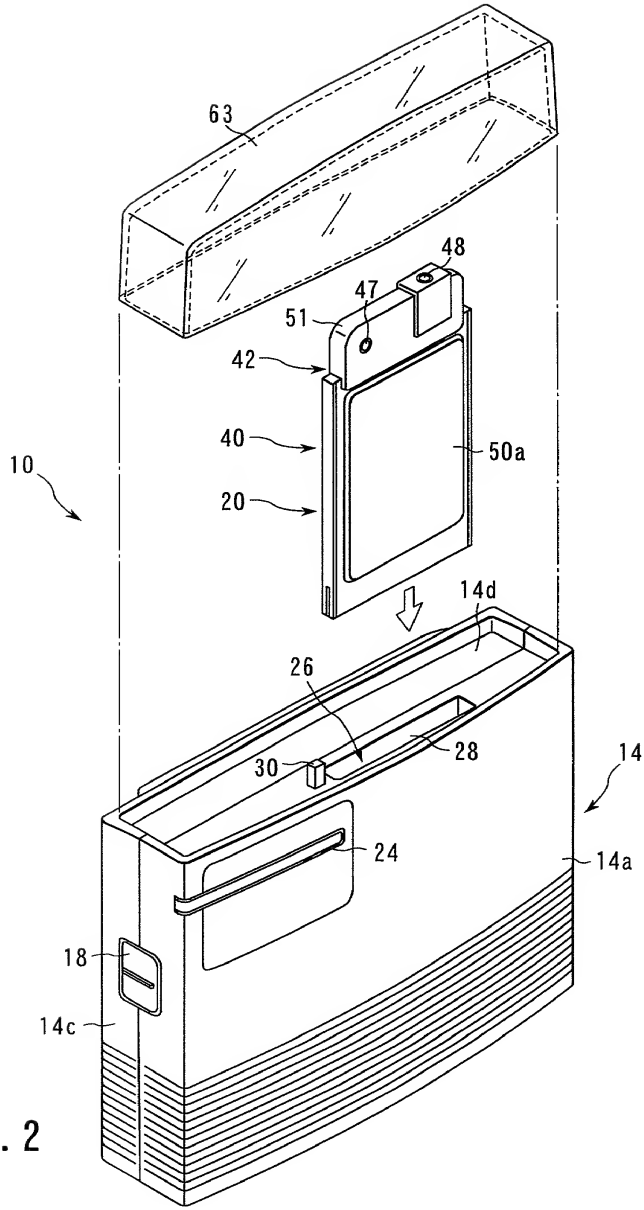

FIG. 2

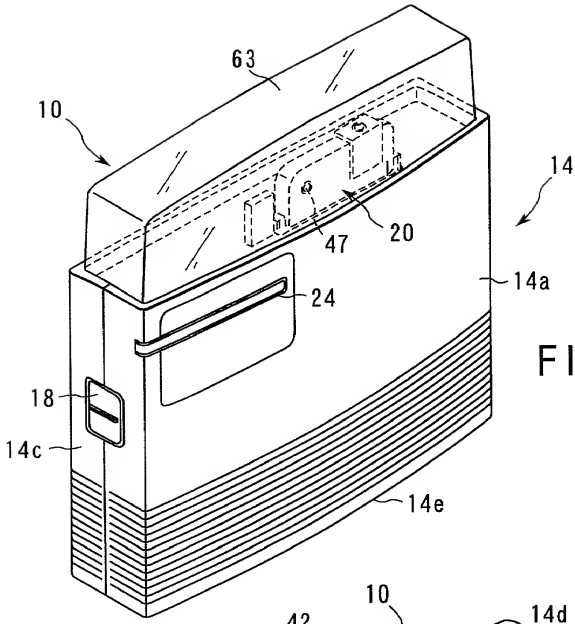
63
10
14
20
47
14a
24
18
14c
14e

FIG. 3

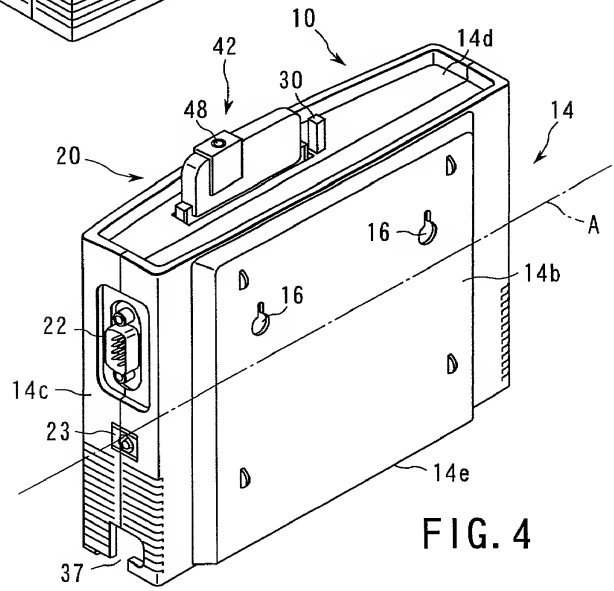
10
14d
42
30
48
14
20
A
16
14b
16
22
14c
23
14e
37

FIG. 4

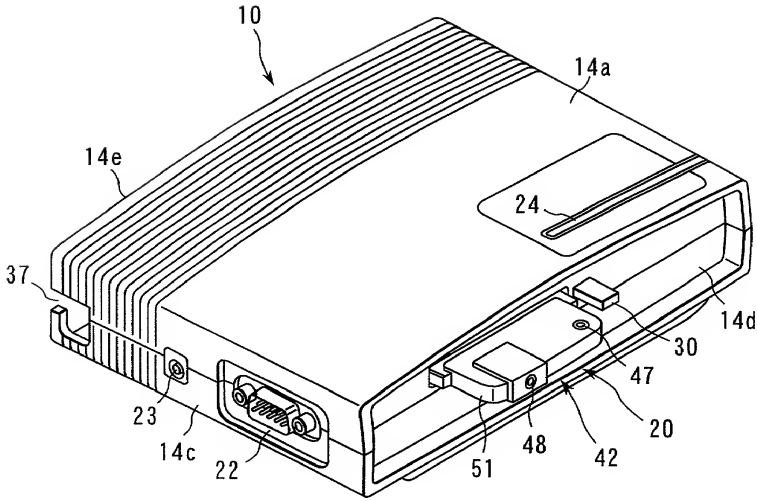
10
14a
14e
24
37
14d
30
47
20
23
14c
22
51
48
42

FIG. 5

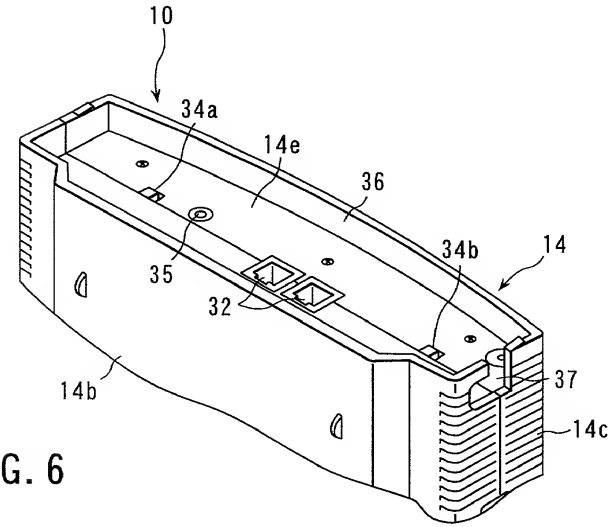
10
34a
14e
36
34b
14
35
32
37
14b
14c

FIG. 6

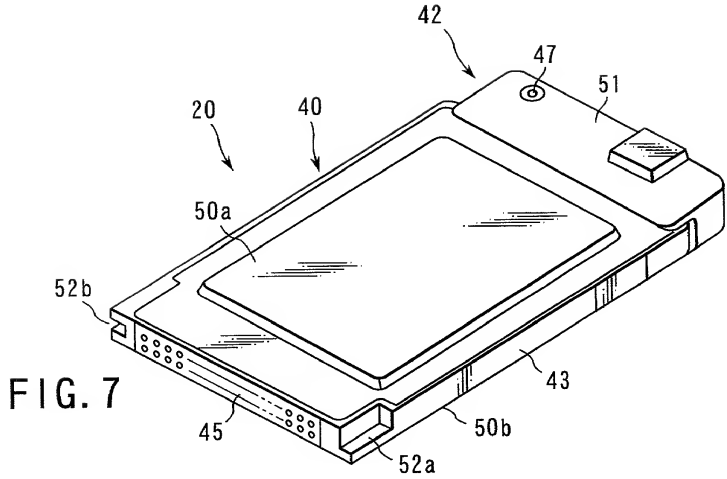
42
47
51
20
40
50a
52b
43
45
50b
52a

FIG. 7

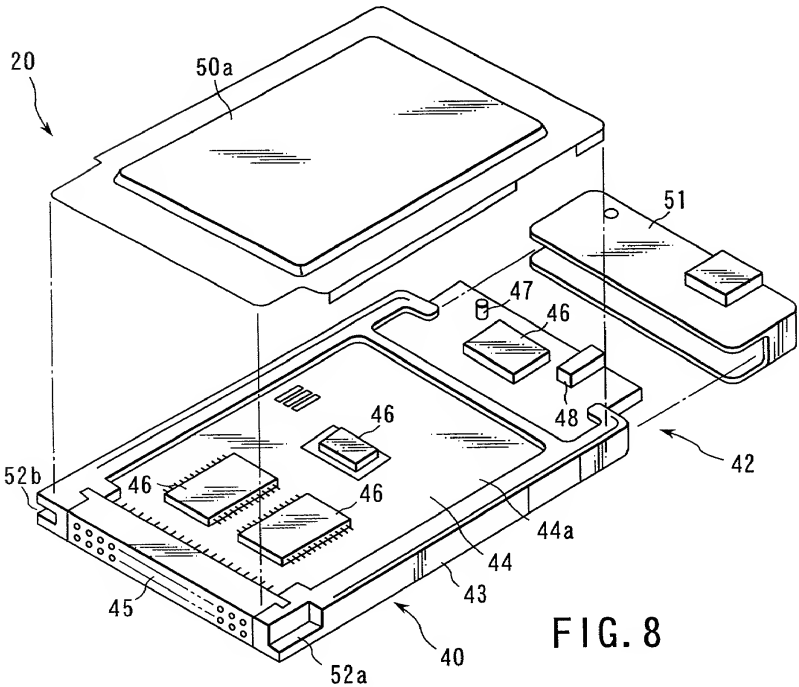
20
50a
51
47
46
48
42
46
52b
46
46
44a
44
43
45
40
52a

FIG. 8

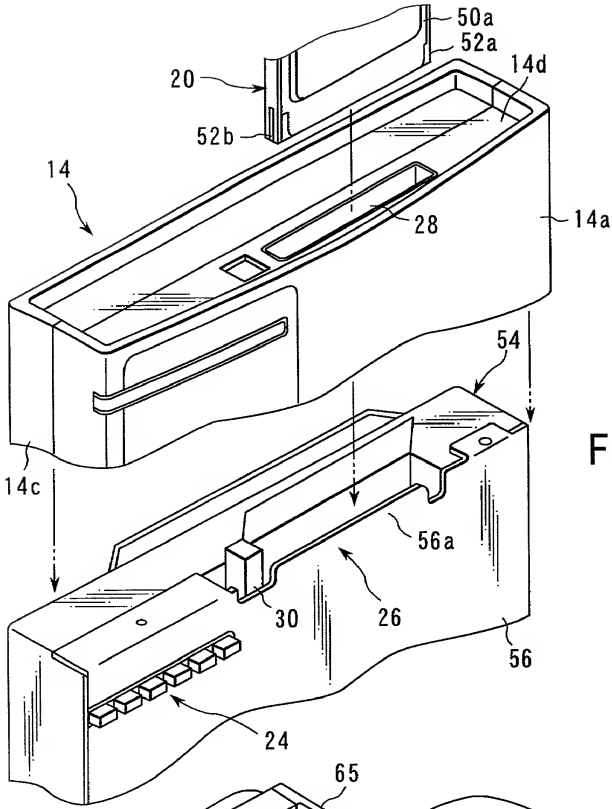
50a
52a
14d
20
52b
14
28
14a
54
14c
56a
30
26
56
24

FIG. 9

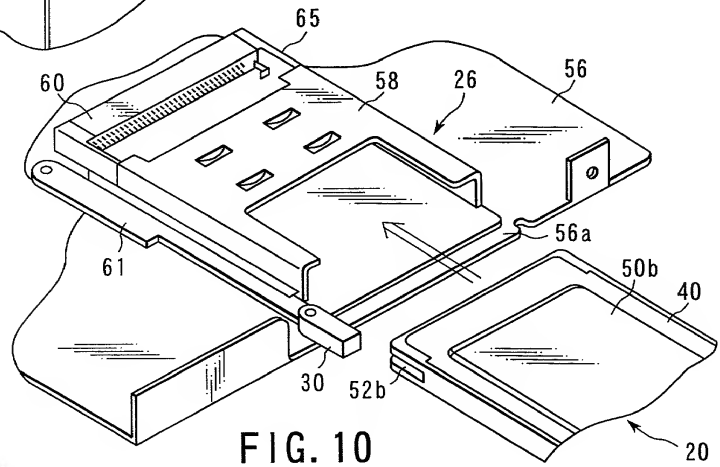
65
60
58
26
56
56a
61
50b
40
30
52b
20

FIG. 10

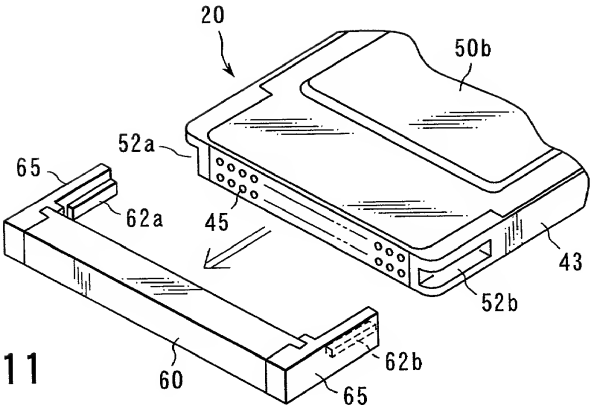

FIG. 11

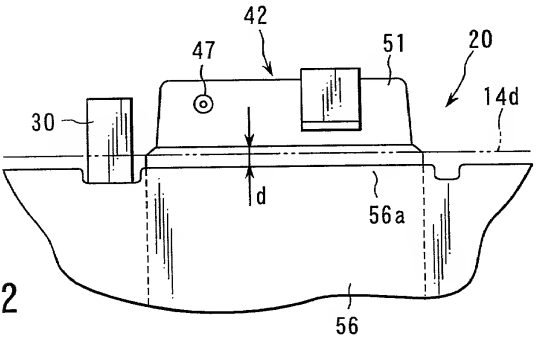

FIG. 12

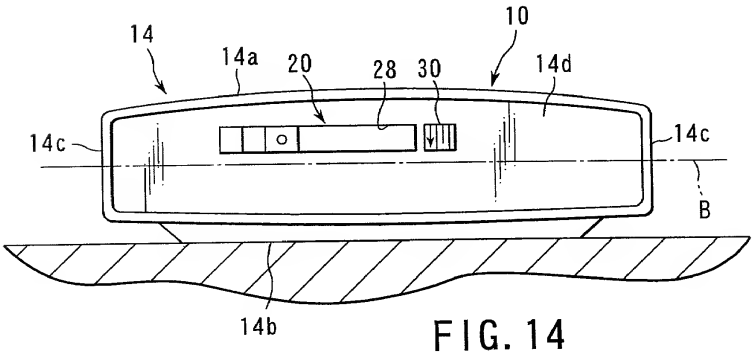

FIG. 14

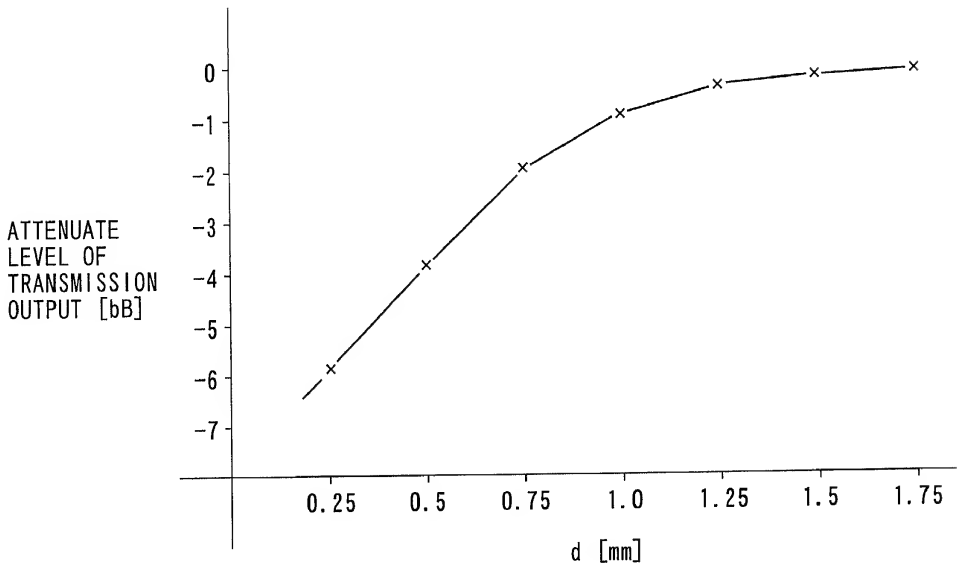
ATTENUATE
LEVEL OF
TRANSMISSION
OUTPUT [bB]
0
-1
-2
-3
-4
-5
-6
-7
0.25
0.5
0.75
1.0
1.25
1.5
1.75
d [mm]

FIG. 13

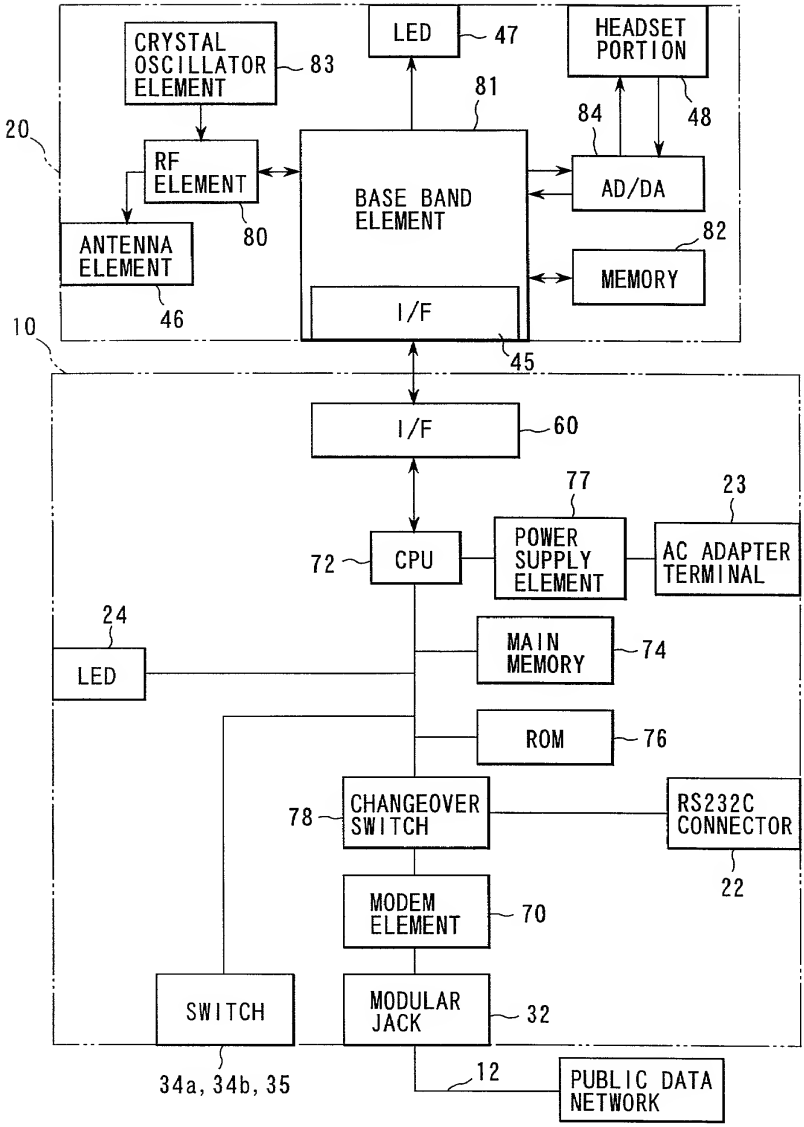
CRYSTAL OSCILLATOR ELEMENT
83
LED
47
HEADSET PORTION
81
84
48
20
RF ELEMENT
80
BASE BAND ELEMENT
AD/DA
ANTENNA ELEMENT
46
82
MEMORY
I/F
45
10
I/F
60
77
23
72
CPU
POWER SUPPLY ELEMENT
AC ADAPTER TERMINAL
24
LED
MAIN MEMORY
74
ROM
76
78
CHANGEOVER SWITCH
RS232C CONNECTOR
22
MODEM ELEMENT
70
SWITCH
MODULAR JACK
32
34a, 34b, 35
12
PUBLIC DATA NETWORK

FIG. 15

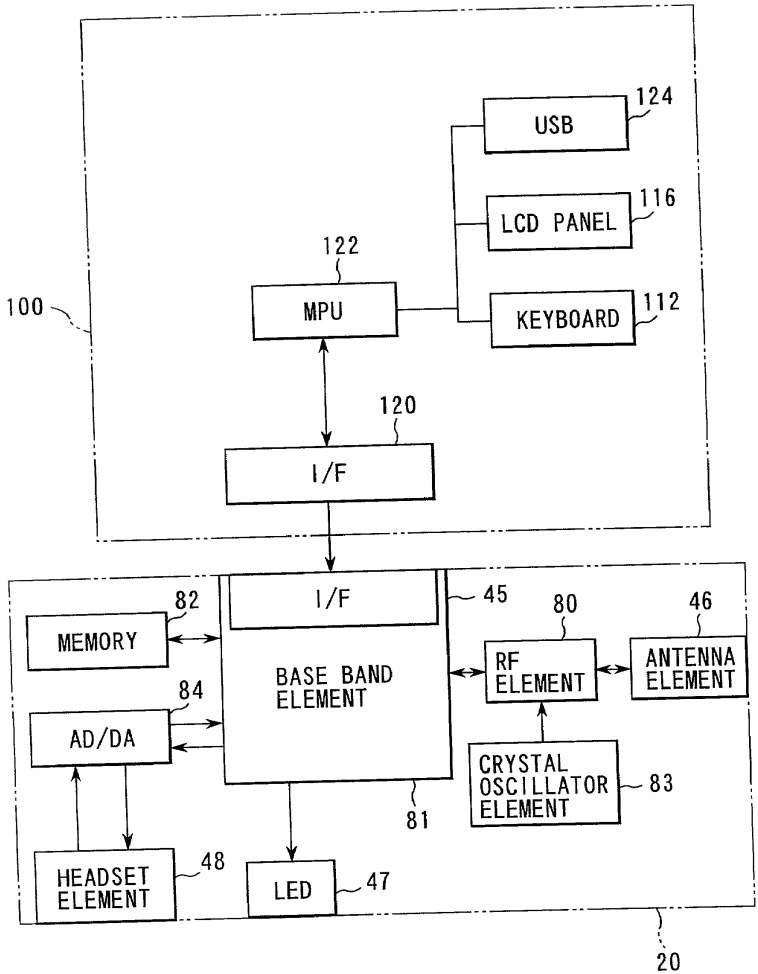
100
USB
124
LCD PANEL
116
122
MPU
KEYBOARD
112
120
I/F
I/F
45
82
MEMORY
80
46
RF ELEMENT
ANTENNA ELEMENT
BASE BAND ELEMENT
84
AD/DA
CRYSTAL OSCILLATOR ELEMENT
83
81
HEADSET ELEMENT
48
LED
47
20

FIG. 16

SETTING OF SLIDE & ROTARY SWITCHES

	OPERATING STATES	SLIDE SW1	SLIDE SW2	ROTARY SWITCH POs.#	1	2	3	4	REMARKS
USER SETTING	NORMAL (MODEM)	L	L	0, 2, 4, 6	L	x	x	L	
	NORMAL (AT)	H	L	0, 2, 4, 6	L	x	x	L	
	MAINTENANCE (MODEM)	L	H	0, 2, 4, 6	L	x	x	L	CPU PROHIBITS INTERRUPTION OF UART SYSTEM
	MAINTENANCE (CPU)	H	H	0, 2, 4, 6	L	x	x	L	PIN CODE CHANGED
SETTING FOR MAINTENANCE OPERATION	INITIALI-ZATION 1	L	L	1, 3, 5, 7	H	x	x	L	EEPROM INITIALIZATION EXECUTED
	INITIALI-ZATION 0	H	L	1, 3, 5, 7	H	x	x	L	EEPROM INITIALIZATION STARTED RESERVED
	RESERVED	L	H	1, 3, 5, 7	H	x	x	L	
	TEST MODE	H	H	1, 3, 5, 7	H	x	x	L	PCB INSPECTION, CPU F/W RELOADING, ETC.
SETTING FOR SHIPMENT	RESERVED	L	L	8	L	x	x	H	
	TCI(HCI)	H	L	8	L	x	x	H	FOR HCI EVALUATION
	RESERVED	L	H	8	L	x	x	H	
	TCI(L2CAP)	H	H	8	L	x	x	H	L2CAP EVALUATION
	RESERVED	L	L	9	H	x	x	H	MODEM-DIR STATE
	RESERVED	H	L	9	H	x	x	H	TA STATE
	RESERVED	L	H	9	H	x	x	H	MODE STATE
	RESERVED	H	H	9	H	x	x	H	TA STATE

FIG. 17